

FIG. 3 Prior Art

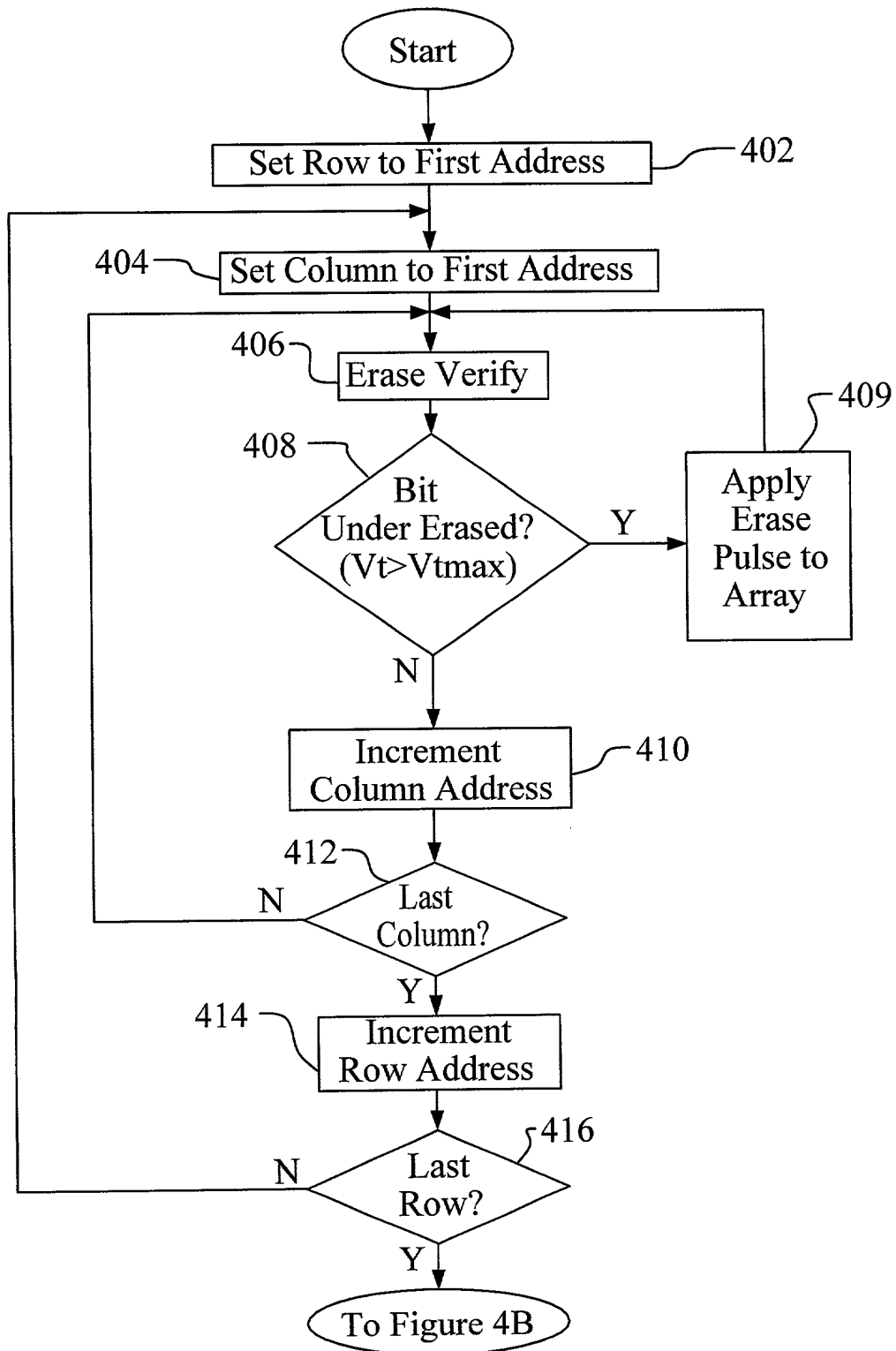
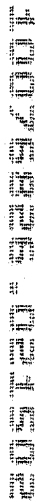


FIG. 4A Prior Art

[illegible]

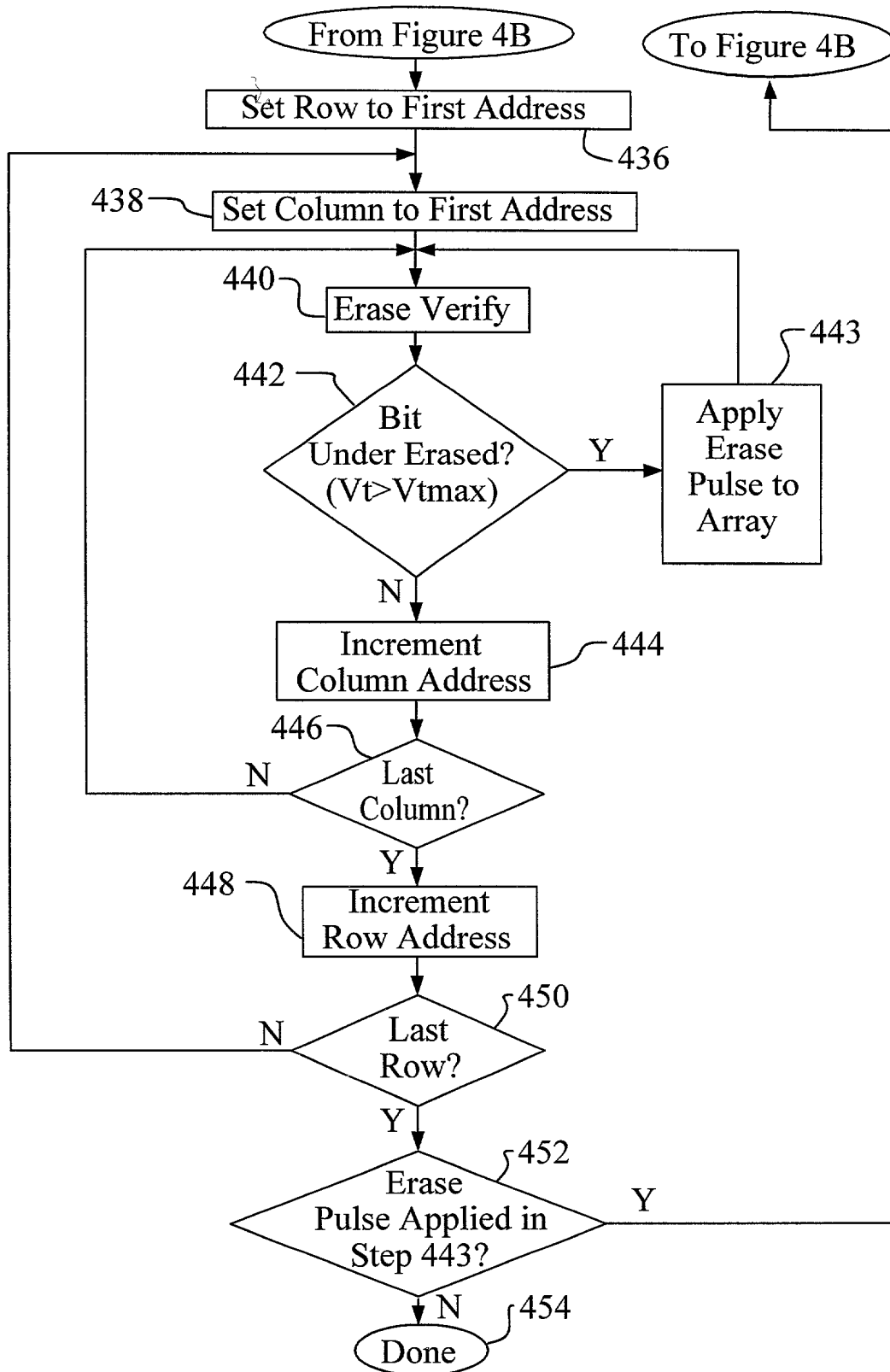


FIG. 4C Prior Art

## ETOX NOR Array (on P-sub)

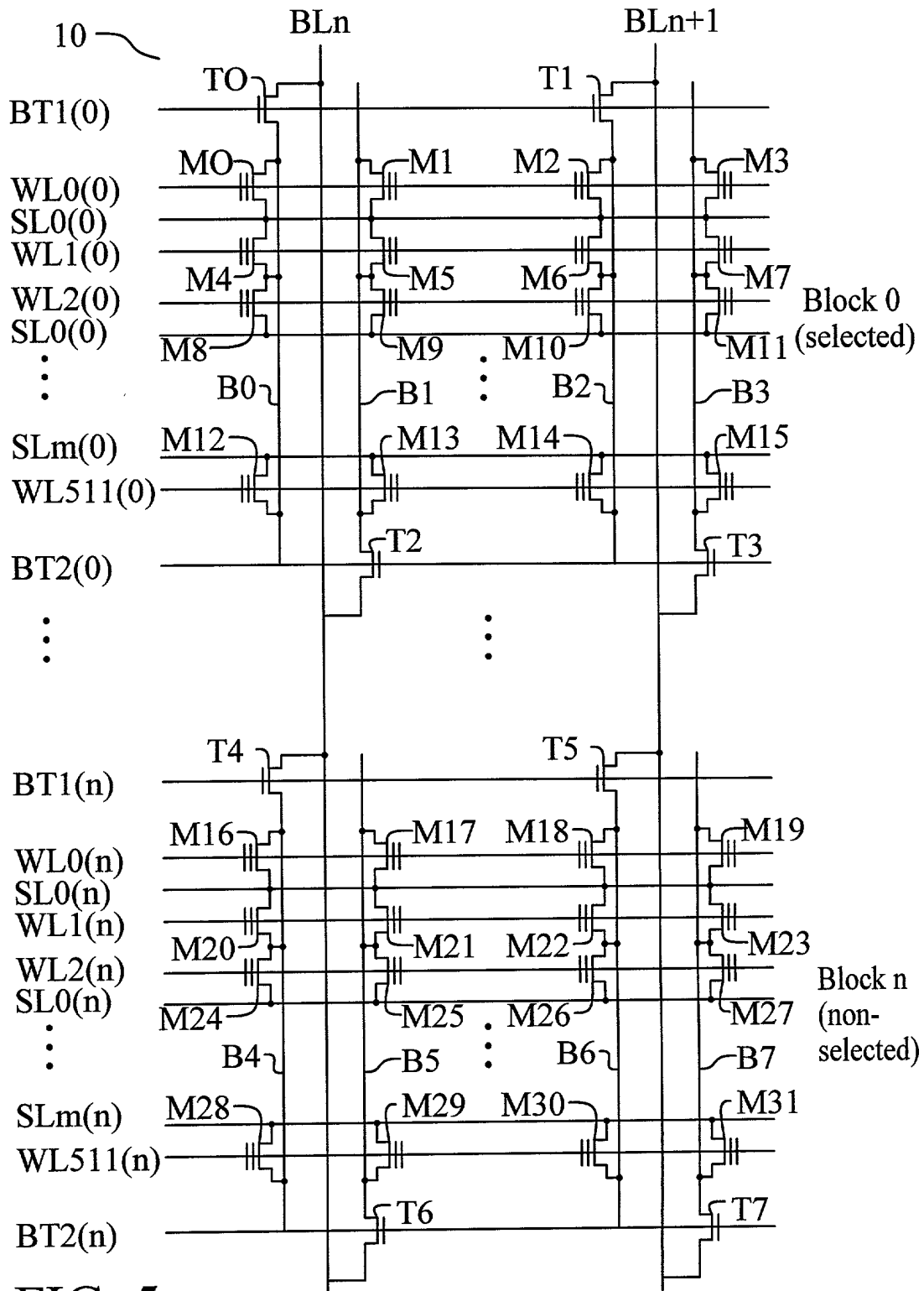


FIG. 5

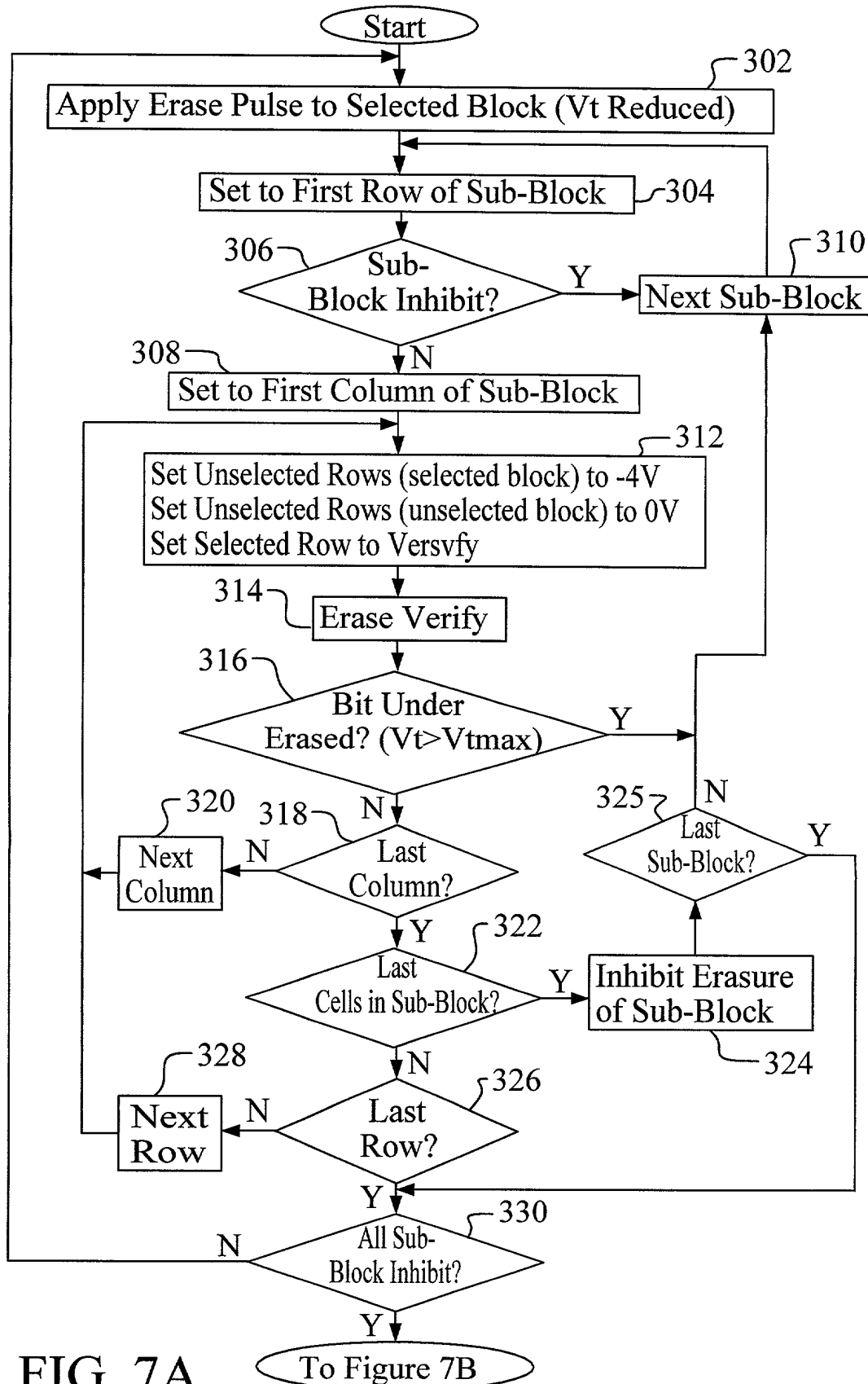
	Erase	Erase Verify*	Erase Inhibit**	Correction Verify***	Correction***
Block 0 (selected)	BLn	0V	0V	0V	0V
	BLn+1	0V	+1V	+1V	+5V
	BT1(0)	0V	0V	0V	0V
	WL0(0)	-10V	Versvfy	0V	0V
	SL0(0)	+5V	0V	0V	0V
	WL1(0)	-10V	-4V	Vcorvfy	Vcorr
	WL2(0)	-10V	-4V	-4V	-4V
	SLm(0)	+5V	0V	0V	0V
	WL511(0)	-10V	-4V	-4V	-4V
	BT2(0)	0V	Vdd	Vdd	+10V
	BT1(n)	0V	0V	0V	0V
	WL0(n)	0V	0V	0V	0V
Block n (non- selected)	SL0(n)	0V	0V	0V	0V
	WL1(n)	0V	0V	0V	0V
	WL2(n)	0V	0V	0V	0V
	SLm(n)	0V	0V	0V	0V
	WL511(n)	0V	0V	0V	0V
	BT2(n)	0V	0V	0V	0V
	BT1(n)	0V	0V	0V	0V
	WL0(n)	0V	0V	0V	0V

Note: \* M3 is selected

\*\* M12, M13, M14 and M15 are selected

\*\*\* M7 is selected; M0, M1, M2 and M3 pass the verification of correction

FIG. 6



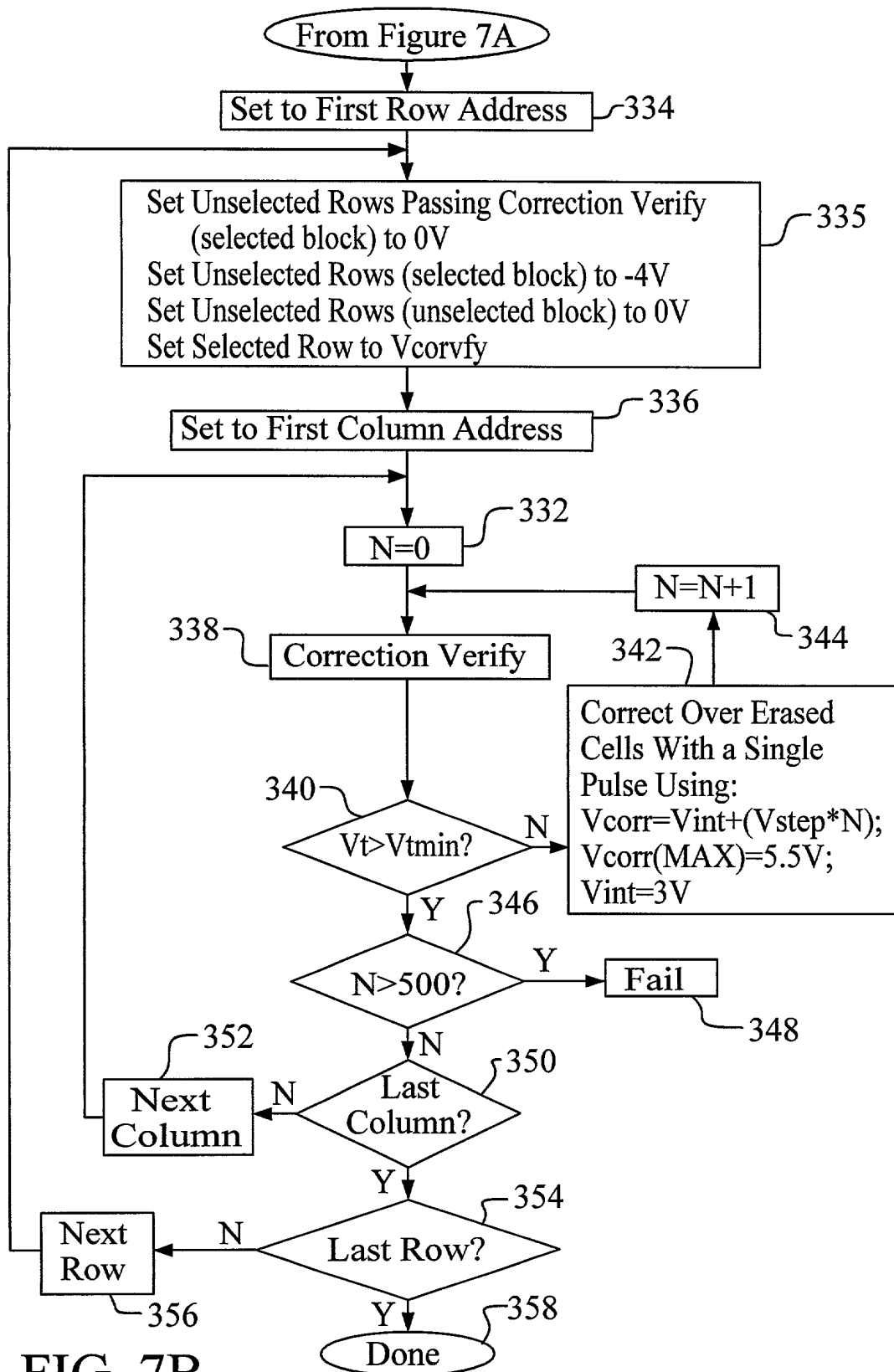


FIG. 7B

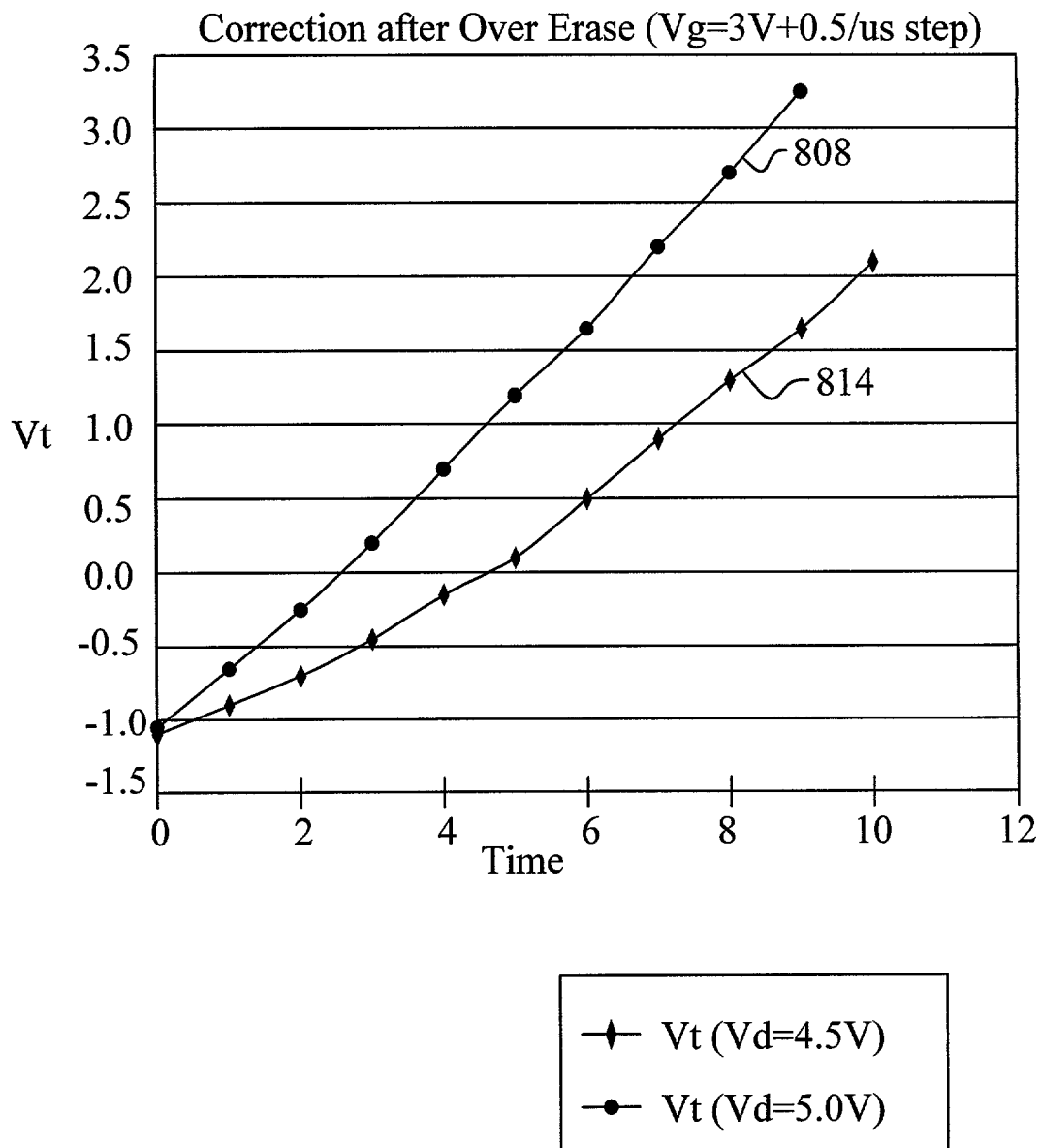


FIG. 8

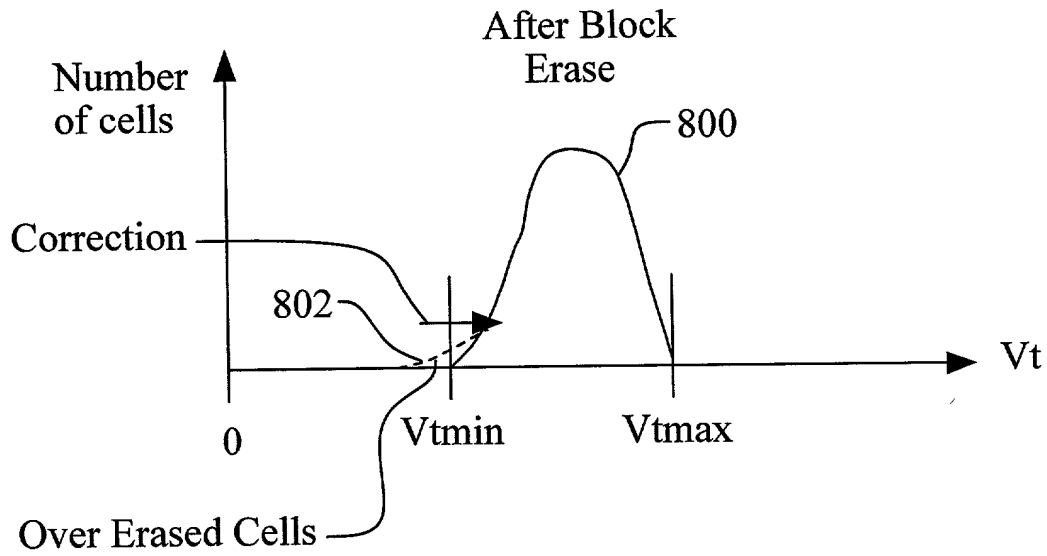


FIG. 9A Prior Art

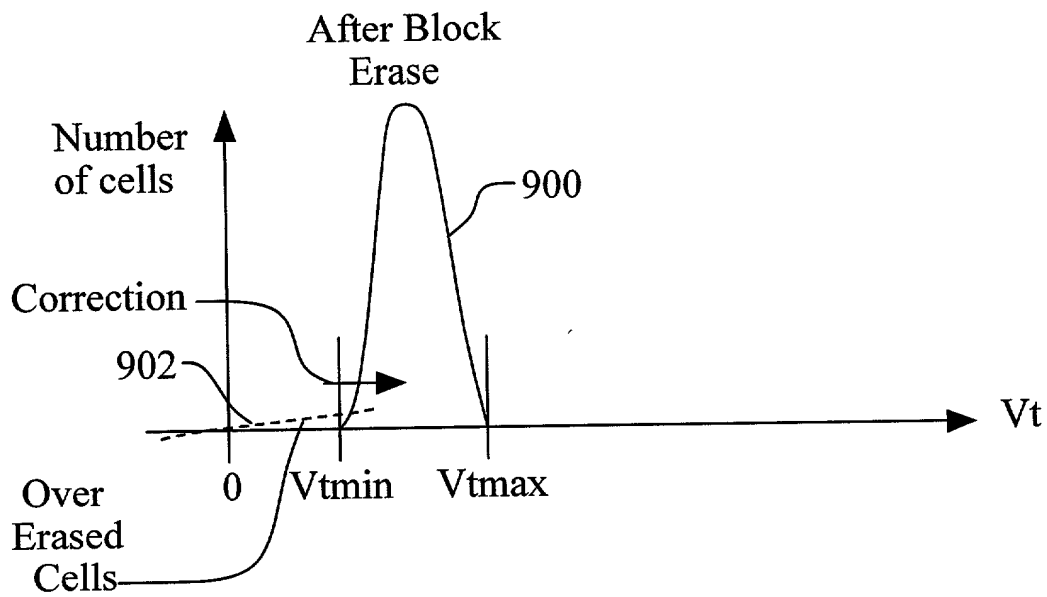


FIG. 9B

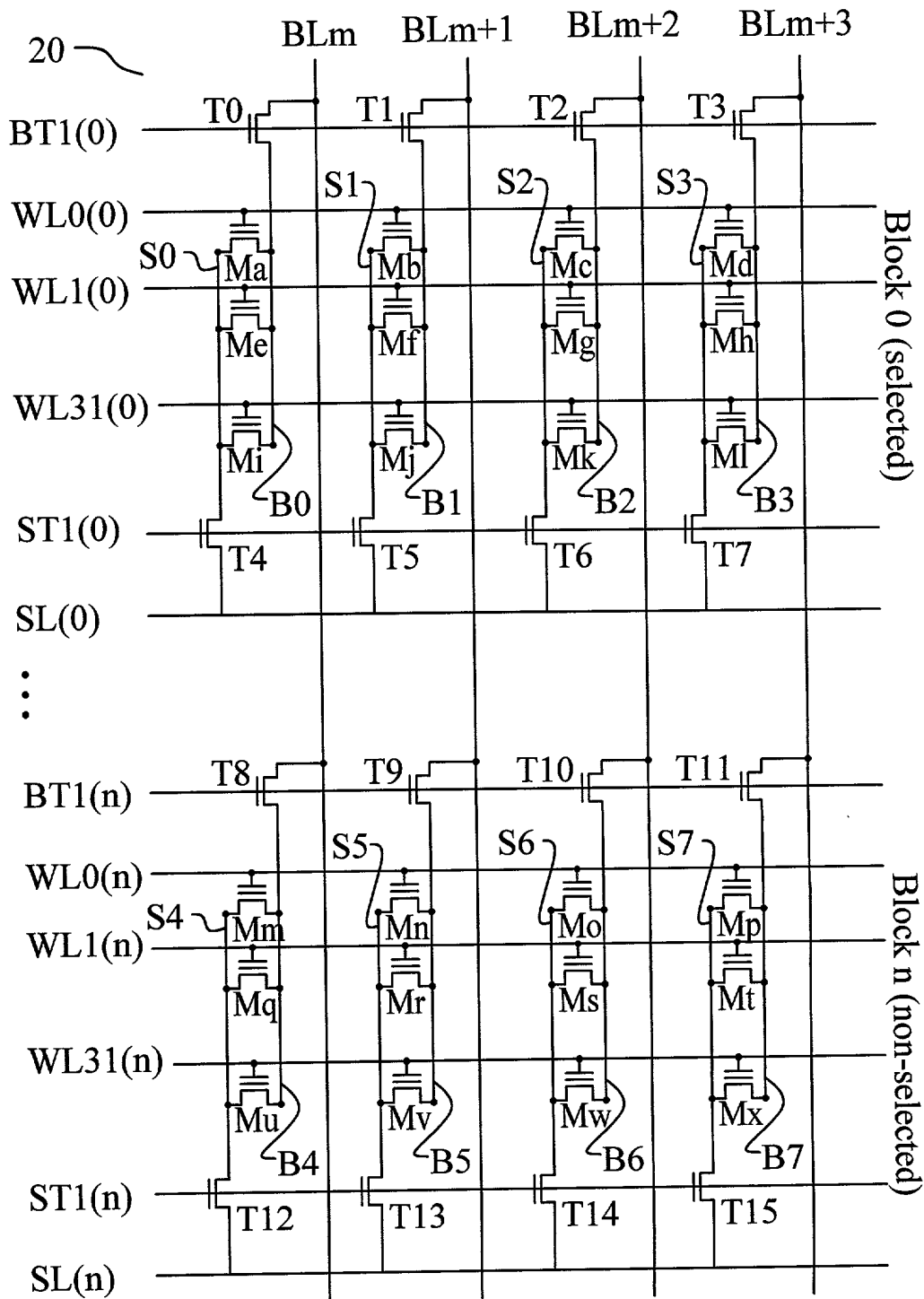


FIG. 10 Prior Art

	Erase	Erase Verify*	Erase Inhibit**	Correction Verify*	Correction***
Block 0 (selected)	BLm	0V	+1V	0V	0V
	BLm+1	0V	+1V	+1V	+5V
	BLm+2	0V	+1V	+1V	0V
	BLm+3	0V	+1V	+1V	+5V
	BT1(0)	Vdd	Vdd	Vdd	+10V
	WL0(0)	-15V	Versvfy	Vcorvfy	Vcorr
	WL1(0)	-15V	-4V	-4V	+2.5V
	WL31(0)	-15V	-4V	-4V	+2.5V
	SL(0)	0V	0V	0V	0V
	ST1(0)	Vdd	Vdd	Vdd	0V
Block n (non- selected)	BT1(n)	0V	0V	0V	0V
	WL0(n)	0V	0V	0V	0V
	WL1(n)	0V	0V	0V	0V
	WL31(n)	0V	0V	0V	0V
	SL(n)	0V	0V	0V	0V
	ST1(n)	0V	0V	0V	0V
		0V	0V	0V	0V

Note: \* Ma, Mb, Mc and Md are selected  
 \*\* Mi, Mj, Mk and Ml are selected  
 \*\*\* Mb and Md are correction inhibit  
 Ma and Mc are corrected

FIG. 11

## Erase Operations

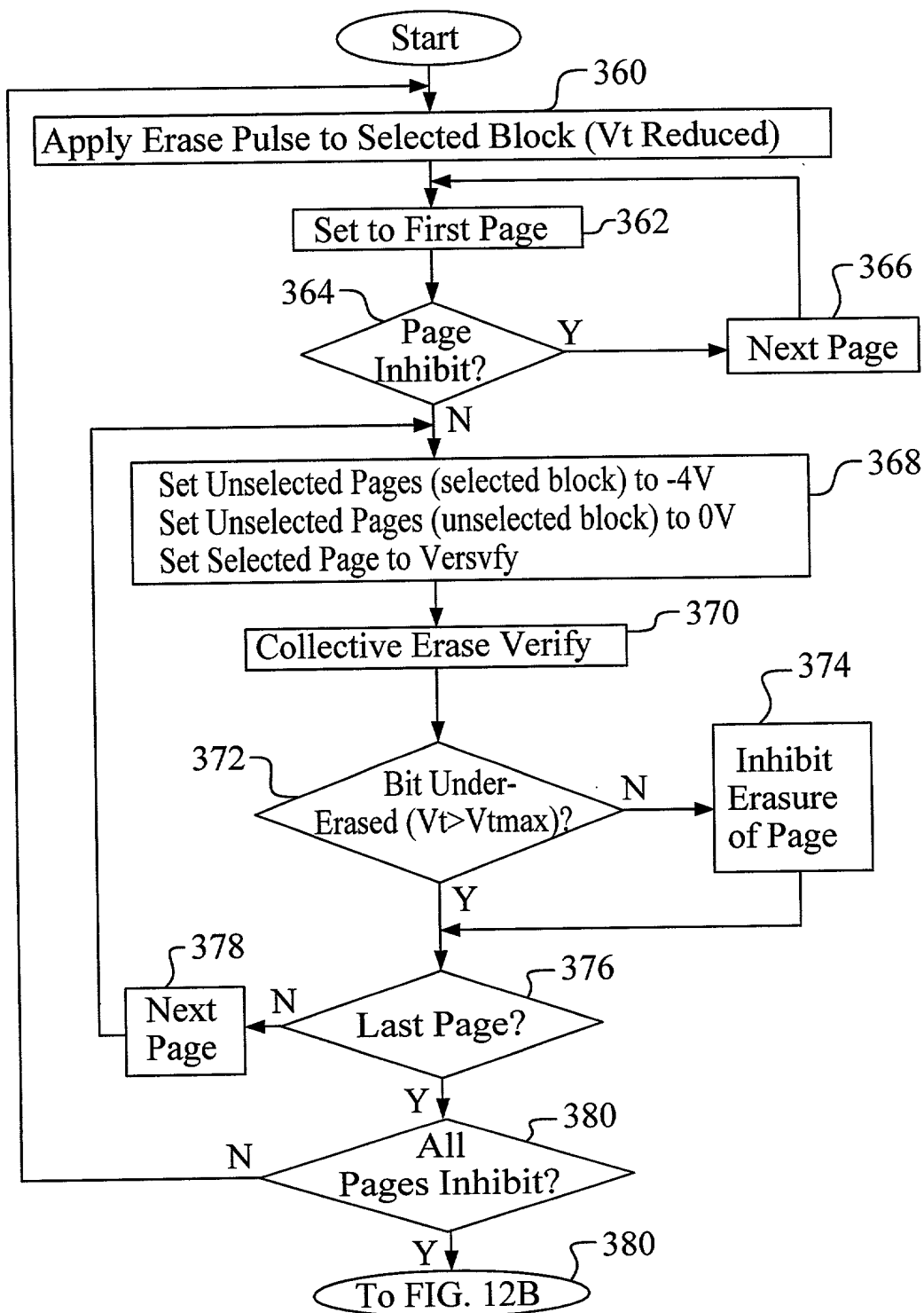


FIG. 12A

## Correction Operations

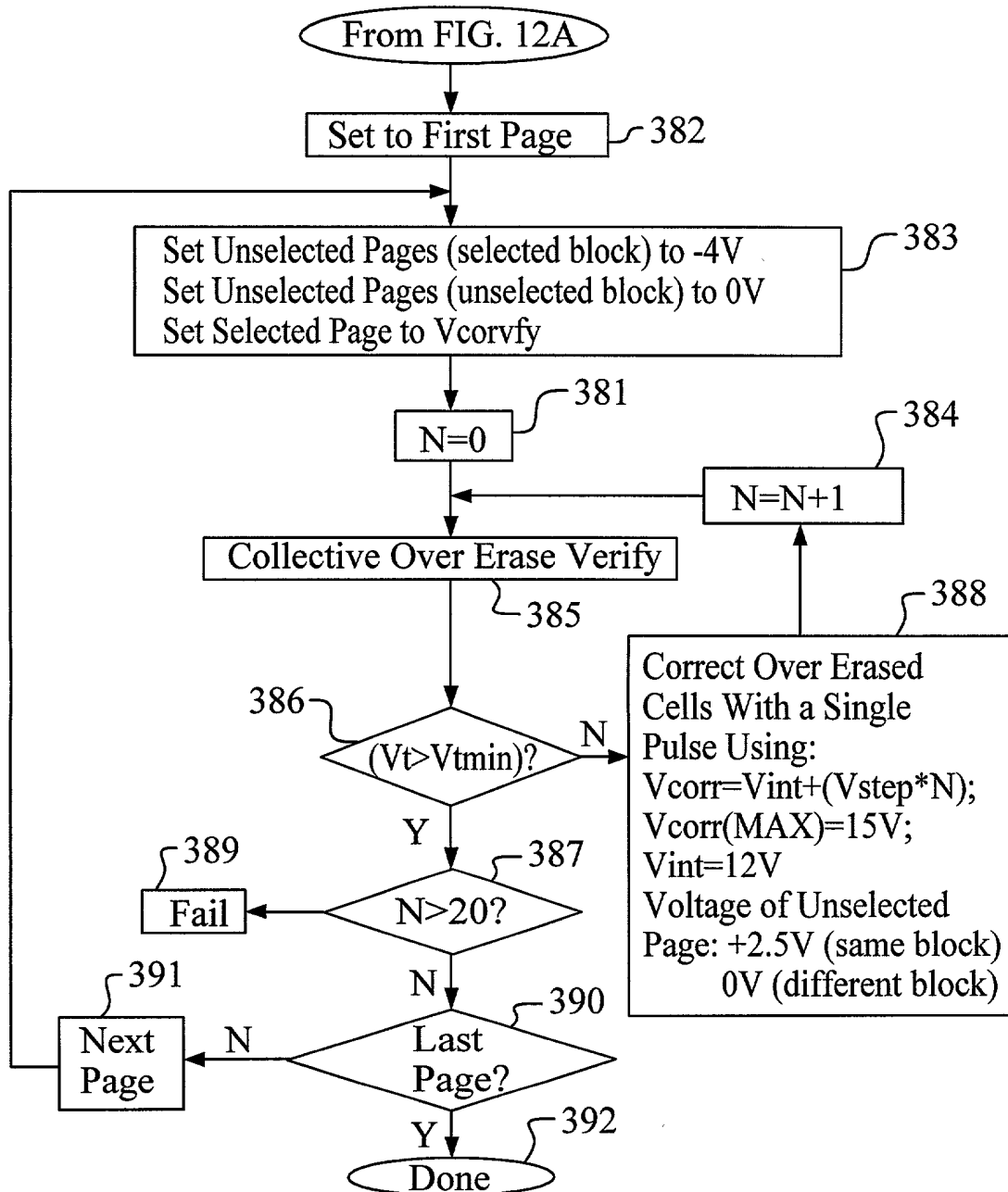


FIG. 12B